Form PTO-1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. ACT-280COA	Serial No. 10/722,636
Information Disclosure Statement by Applicant	Applicant: Plants et al.	
(Use several sheets if necessary)	Filed: November 25, 2003 Group: 2185	

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	1	5,666,322	09/09 /1997	Conkle	365	233	09/21/1995
	2	5,994,934	11/30/1999	Yoshimura et al.	327	158	07/08/1998
	3	6,043, 677	03/28/2000	Albu et al.	326	39	10/15/1997
	4	6,111,448	08/29/2000	Shibayama	327	293	09/10/1998
	5	6,181,174 B1	01/30/2001	Fujieda et al.	327	158	09/23/1999
	6	6,289,068 B1	09/11/2001	Hassoun et al.	375	376	06/22/1998
	7	6,292,016 B1	09/18/2001	Jefferson et al.	326	39	06/05/2000
	8	6,437,650 B1	08/20/2002	Sung et al.	331	25	05/15/2001

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No
	9	EP 1 137 188 A2	09/26/2001	Europe	H03L	07/08		X
	10	EP 1 137 188 A3	08/13/2003	Europe	H03L	07/08		X

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

	11	L. Ashby, "ASIC Clock Distribution us a Phase Locked Loop (PLL)", Proceedings Fourth Annual IEEE International ASIC Conference and Exhibit, pp. 6.1-6.3, September 1991.
	12	"AV9170 Application Note: Clock Synchronizer and Multiplier" AvaSem Corp, pp. 1-8, November 1992
	13	AV9170 Application Note Preliminary Information, AvaSem, pp. 1-6, January 1993
	14	U. Shannon et al., "A 30-ps JITTER, 3.6 us Locking, 3.3-Volt Digital PLL for CMOS Gate Arrays", IEEE 1993 Custom Integrated Circutis Conference, pp. 23.3.1-23.3.4, Conf. Date: May 9-12, 1993.
	15	A. Efendovich et al., "Multi-Frequency Zero-Jitter Delay-Locked Loop", IEEE 1993 Custom Intedgrated Circuits Conference, pp. 27.1.1-27.1.4, Conf Dte: May 9-12, 1993.
	16	R. Quinnell, "Blending gate arrays with dedicaed circuits sweetens ASIC development", EDN, pp. 29-32, March 31, 1994.
	17	J. Chen, "PLL-based clock systems span the system spectrum from green PCs to Alpha", EDN, pp. 147-155, November 9, 1995.
	18	P. Sevalia, "Straightforward technicques cut jitter in PLL-based clock drives", EDN, pp. 119-125, November 23, 1995.
	19	D. Bursky, "Memories Hit New Highs And Clocks Run Jitter-Free", Electronic Design, pp. 79-93, February 19, 1996.

Examiner	Date Considered 6/10/04

Examiner: Initial if citation considered, whether or not citation is in conference with MPEP 609; Draw line through citation if not conformance and not considered. Include a copy of this form with the next communication to applicant.